- Types of bus cycles:
  - **Memory Read Bus Cycle**
  - **Memory Write Bus Cycle**
  - **Input/Output Read Bus Cycle**
  - **Input/Output Write Bus Cycle**
- The **bus cycle** of the 8086 microprocessor consists of **at least four clock periods**. These four time states are called **T_1, T_2, T_3 and T_4**.

8.11 MEMORY READ AND WRITE BUS CYCLES

- **Fig. 8-22(a)** shows a **memory read cycle** of the **8086**:
- During **period T_1**,
  - The 8086 outputs the **20-bit address** of the memory location to be accessed on its multiplexed **address/data bus**. $\overline{\mathbf{BHE}}$ is also output along with the address during T_1.
  - At the same time a pulse is also produced at **ALE**. The **trailing edge** or the **high level** of this pulse is used to **latch** the address in external circuitry.
  - Signal **M/$\overline{\mathbf{IO}}$** is set to **logic 1** and signal **DT/$\overline{\mathbf{R}}$** is set to the **0 logic level** and both are maintained throughout all four periods of the bus cycle.
- Beginning with **period T_2**,
  - Status bits **S_3** through **S_6** are output on the upper four address bus lines. This status information is maintained through periods **T_3** and **T_4**.
  - On the other hand, address/data bus lines **AD_0 through AD_7** are put in the **high-Z state** during **T_2**.
  - Late in period **T_2**, $\overline{\mathbf{RD}}$ is switched to **logic 0**. This indicates to the memory subsystem that a read cycle is in progress. $\overline{\mathbf{DEN}}$ is switched to **logic 0** to enable external circuitry to allow the data to move from memory onto the microprocessor's data bus.
- During **period T_3**,
  - The memory must provide **valid data** during **T_3** and maintain it until after the processor terminates the read operation. The data read by the 8086 microprocessor can be carried over all **16 data bus** lines

- During **T_4,**
    - The 8086 switches $\overline{\textbf{RD}}$ to the inactive **1 logic level** to terminate the read operation. $\overline{\textbf{DEN}}$ returns to its inactive logic level late during **T_4** to disable the external circuitry.
- **Fig. 8-22(b)** shows a **memory write cycle** of the 8088:
- During **period T_1,**
    - The **address** along with $\overline{\textbf{BHE}}$ are output and latched with the **ALE** pulse.
    - **M/$\overline{\textbf{IO}}$** is set to **logic 1** to indicate a memory cycle.
    - However, this time **DT/$\overline{\textbf{R}}$** is switched to **logic 1**. This signals external circuits that the 8086 is going to **transmit data** over the bus.
- Beginning with **period T_2,**
    - $\overline{\textbf{WR}}$ is switched to **logic 0** telling the memory subsystem that a write operation is to follow.
    - The 8086 puts the **data** on the bus late in **T_2** and maintains the data valid through **T_4**. Data will be carried over all **16 data bus lines**.
    - $\overline{\textbf{DEN}}$ enables the external circuitry to provide a path for data from the processor to the memory.

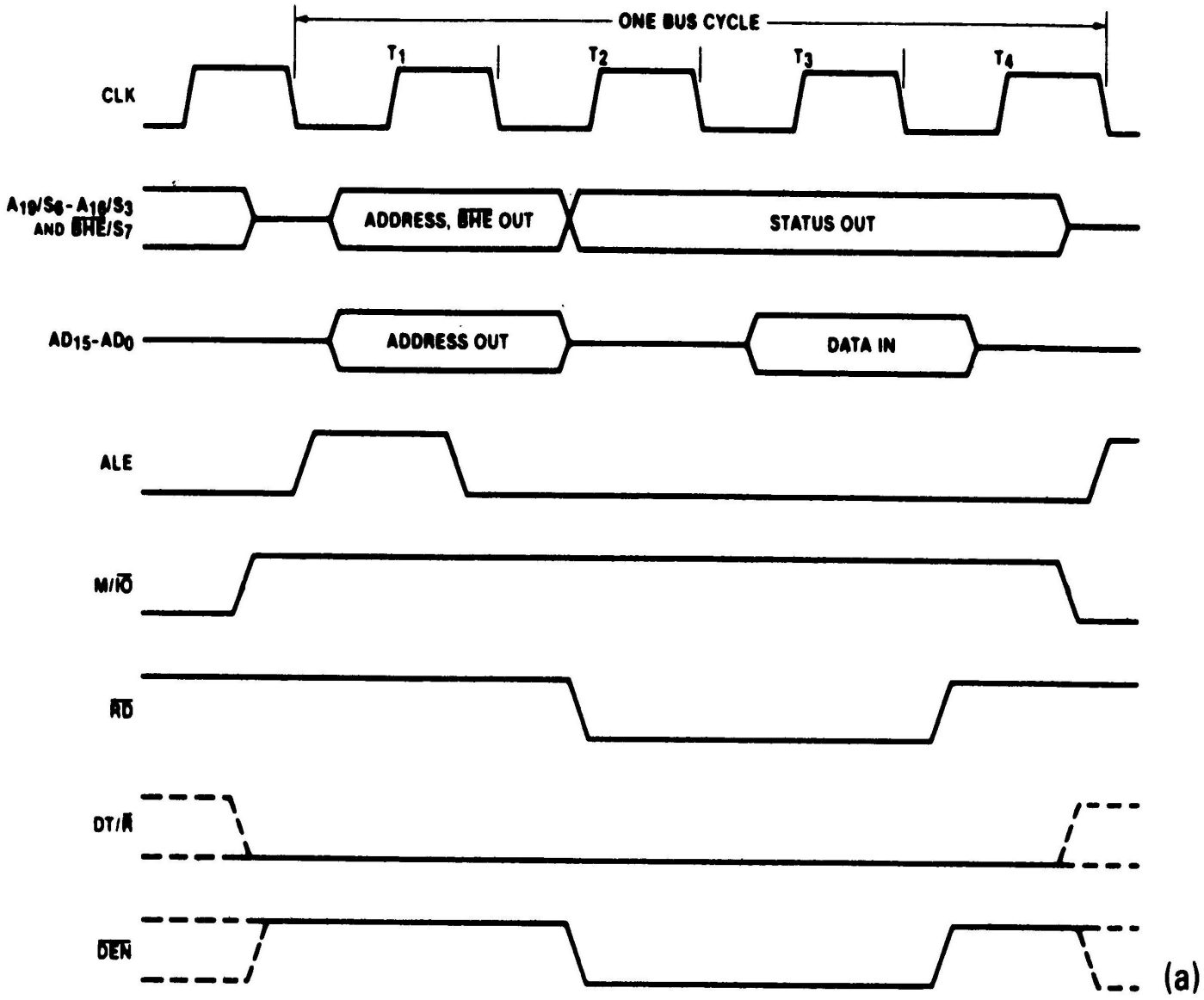

Figure 8-22(a) Minimum-mode memory read bus cycle of the 8086.

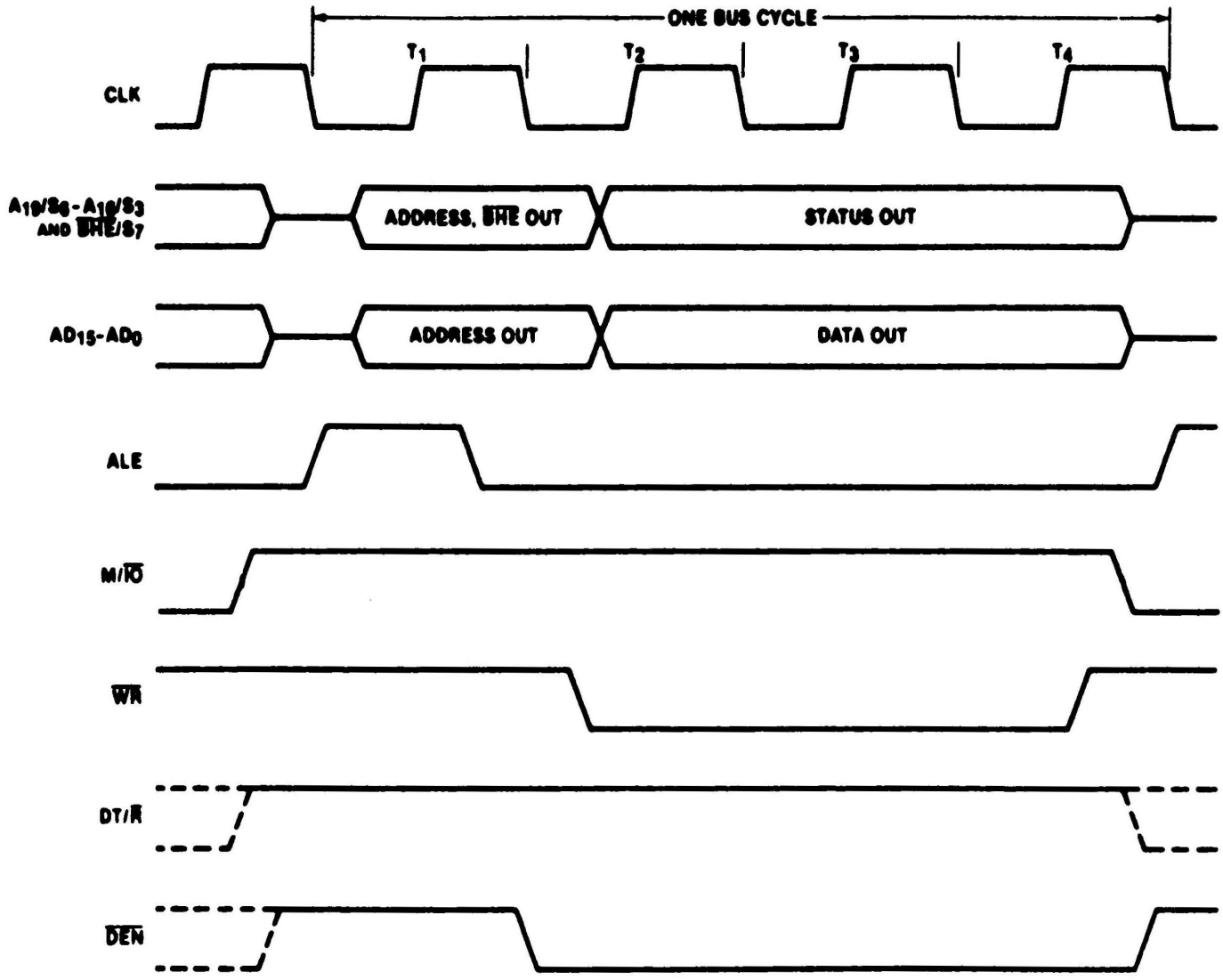

Figure 8-22(b) Minimum-mode memory write bus cycle of the 8086.

8.8 HARDWARE ORGANIZATION OF MEMORY ADDRESS SPACE

- The memory address space of the 8086-based microcomputers has different logical and physical **organizations** (see **Fig. 8-15**).
- **Logically**, memory is implemented as a single **1M × 8 memory chunk**. The byte-wide storage locations are assigned consecutive addresses over the range from 00000_{16} through $FFFFF_{16}$.
- **Physically**, memory is implemented as **two** independent **512Kbyte banks**: the **low (even) bank** and the **high (odd) bank**. Data bytes associated with an even address (00000_{16}, 00002_{16}, etc.) reside in the low bank, and those with odd addresses (00001_{16}, 00003_{16}, etc.) reside in the high bank.
- Address bits A_1 through A_{19} select the storage location that is to be accessed. They are applied to both banks in parallel. $\mathbf{A_0}$ and bank high enable ($\overline{\mathbf{BHE}}$) are used as **bank-select** signals.

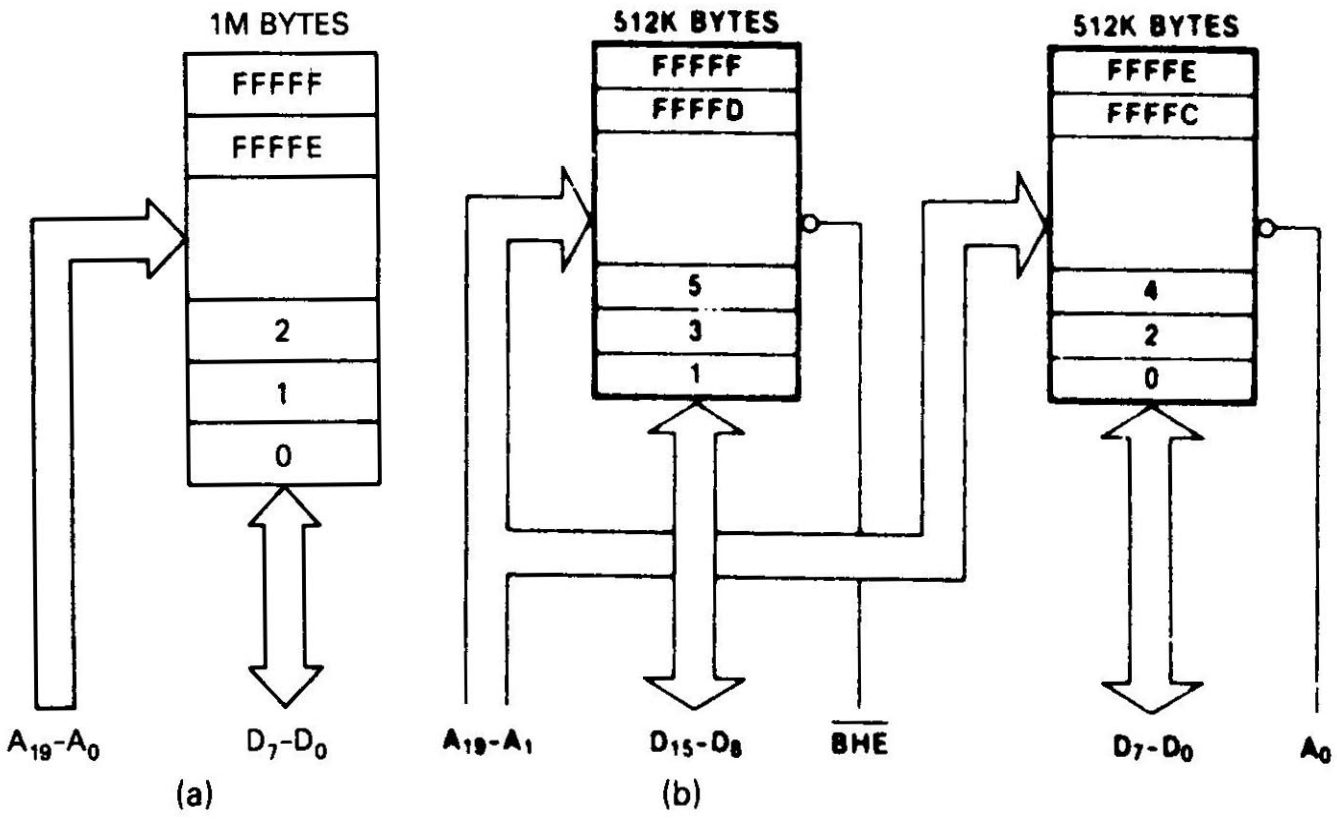

Figure 8-15 (a) Logical memory organization, and (b) Physical memory organization (high and low memory banks) of the 8086 microprocessor.

- **Each** of the memory **banks** provides half of the 8086's 16-bit data bus. The **lower** bank transfers bytes of data over data lines **D_0 through D_7**, while data transfers for a **high** bank use **D_8 through D_{15}**.
- The **8086 microprocessor** accesses memory as follows:
- **Fig. 8-17(a)** shows how a **byte-memory** operation is performed to **address X**, an **even**-addressed storage location. **A_0** is set to **logic 0** to enable the low bank of memory and $\overline{\mathbf{BHE}}$ to **logic 1** to disable the high bank. **Data** are transferred to or from the lower bank over data bus lines **D_0 through D_7**.
- **Fig. 8-17(b)** shows how a **byte-memory** operation is performed to an **odd**-addressed storage location such as **X + 1**. **A_0** is set to **logic 1** and $\overline{\mathbf{BHE}}$ to **logic 0**. This enables the high bank of memory and disables the low bank. Data are transferred over bus lines **D_8** through **D_{15}**. **D_8** represents the **LSB**.
- **Fig. 8-17(c)** illustrates how an **aligned word** (at even address X) is accessed. **Both** the high and low **banks** are accessed at the **same time**. Both **A_0** and $\overline{\mathbf{BHE}}$ are set to 0. This 16-bit word is transferred over the complete data bus **D_0** through **D_{15}** in just **one bus cycle**.
- **Fig. 8-17(d)** illustrates how a **misaligned word** (at address X + 1) is accessed. **Two bus cycles** are needed. During the first bus cycle, the byte of the word located at address X + 1 in the high bank is accessed over **D_8** through **D_{15}**. Even though the data transfer uses data lines **D_8** through **D_{15}**, to the processor it is the **low byte** of the addressed data word. In the **second memory bus cycle**, the even byte located at X + 2 in the low bank is accessed over bus lines **D_0** through **D_7**.