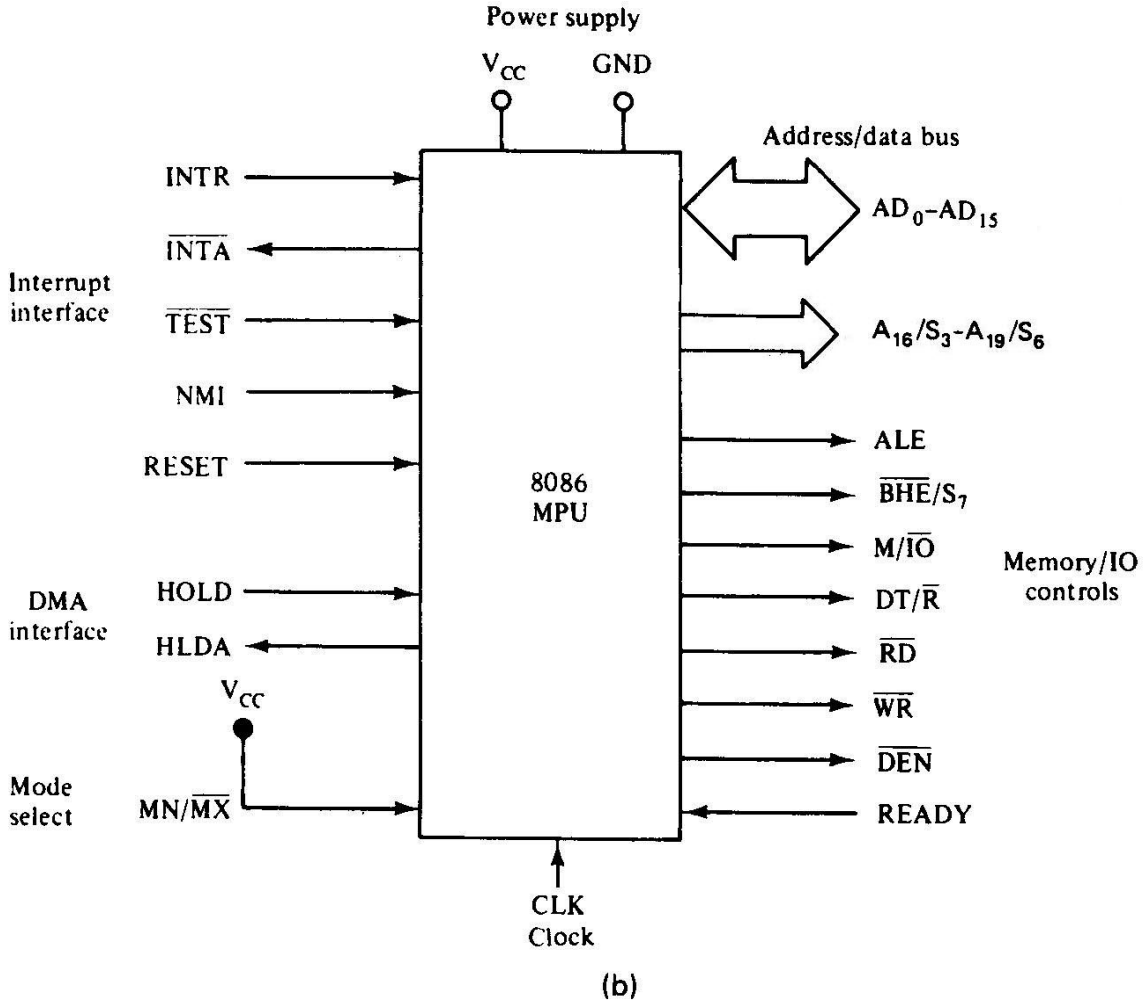

Figure 8–3 (a) Block diagram of the minimum-mode 8088 MPU. (b) Block diagram of the minimum-mode 8086 MPU.

8.3 SUMMARY OF MINIMUM-MODE INTERFACE SIGNALS

- **Address/Data Bus:** The address bus is **20 bits long** and consists of signal lines $\mathbf{A_0}$ (LSB) through $\mathbf{A_{19}}$ (MSB). However, only address lines $\mathbf{A_0}$ through $\mathbf{A_{15}}$ are used when accessing **I/O**.

- The **data bus** lines are **multiplexed** with address lines. For this reason, they are denoted as $\mathbf{AD_0}$ through $\mathbf{AD_{15}}$. Data line $\mathbf{D_0}$ is the LSB.

- **Status Signals:** The four most significant address lines $\mathbf{A_{16}}$ through $\mathbf{A_{19}}$ of the 8086 are multiplexed with **status signals** $\mathbf{S_3}$ through $\mathbf{S_6}$. These status bits are output on the bus at the same time that data are transferred over the other bus lines.

- **Control Signals:**
- When ***Address latch enable*** (**ALE**) is **logic 1** it signals that a **valid address** is on the bus. This address can be latched in external circuitry on the **1-to-0 edge** of the pulse at ALE.
- **M/$\overline{\text{IO}}$** (*memory*/IO) tells external circuitry whether a memory or I/O transfer is taking place over the bus. **Logic 1** signals a **memory operation** and **logic 0** signals an **I/O operation**.
- **DT/$\overline{\text{R}}$** (*data transmit/receive*) signals the **direction of data transfer** over the bus. **Logic 1** indicates that the bus is in the **transmit mode** (i.e., data are either written into memory or to an I/O device). **Logic 0** signals that the bus is in the **receive mode** (i.e., reading data from memory or from an input port).
- The *bank high enable* (**$\overline{\text{BHE}}$**) signal is used as a **memory enable signal** for the **most significant byte** half of the data bus, $\mathbf{D_8}$ through $\mathbf{D_{15}}$.
- **$\overline{\text{WR}}$** (*write*) is switched to **logic 0** to signal external devices that **valid output data** are on the bus.
- **$\overline{\text{RD}}$** (*read*) indicates that the MPU is performing a **read of data** off the bus. During read operations, one other control signal, **$\overline{\text{DEN}}$** (*data enable*), is also supplied. It enables external devices to supply data to the microprocessor.
- The **READY** signal can be used to **insert wait states** into the bus cycle so that it is extended by a number of clock periods. This signal is supplied by a **slow memory or I/O subsystem** to signal the MPU when it is ready to permit the data transfer to be completed.
- **Interrupt Signals:**
- *Interrupt request* (**INTR**) is an **input** to the 8086 that can be used by an **external device** to **signal** that it needs to be **serviced**. **Logic 1** at INTR represents an active interrupt request.
- When the MPU **recognizes an interrupt request**, it indicates this fact to external circuits with logic 0 at the *interrupt acknowledge* (**INTA**) output.
- On the **0-to-1 transition** of *nonmaskable interrupt* (**NMI**), control is passed to a nonmaskable **interrupt service routine** at completion of execution of the current instruction. NMI is the interrupt request with highest priority and **cannot be masked by software**.

- The **RESET** input is used to provide a **hardware reset** for the MPU. Switching RESET to **logic 0** initializes the internal registers of the MPU and initiates a reset service routine.
- **DMA Interface Signals:**
- When an **external device** wants to **take control** of the **system bus**, it signals this fact to the MPU by switching HOLD to the **logic level 1**.
- When in the hold state, lines $\mathbf{AD_0}$ through $\mathbf{AD_{15}}$, $\mathbf{A_{16}/S_3}$ through $\mathbf{A_{19}/S_6}$, $\overline{\mathbf{BHE}}$, $\mathbf{M/\overline{IO}}$, $\mathbf{DT/\overline{R}}$, $\overline{\mathbf{WR}}$, $\overline{\mathbf{RD}}$, $\overline{\mathbf{DEN}}$ and **INTR** are all put in the **high-Z** state. The MPU signals external devices that it is in this state by switching **HLDA** to **1**.

8.6 SYSTEM CLOCK

- To **synchronize** the internal and external operations of the microprocessor a *clock* (**CLK**) **input signal** is used. The CLK can be generated by the **8284 clock generator IC**.
- The **8086** is manufactured in three speeds: **5 MHz**, **8 MHz** and **10 MHz**.
- For **8086**, we connect either a **15-, 24- or 30-MHz crystal** between inputs X_1 and X_2 inputs of the clock chip (see Fig. 8-11). The *fundamental crystal frequency* is **divided by 3** within the 8284 to give either a **5-, 8- or 10-MHz** clock signal, which is directly connected to the CLK input of the 8086.

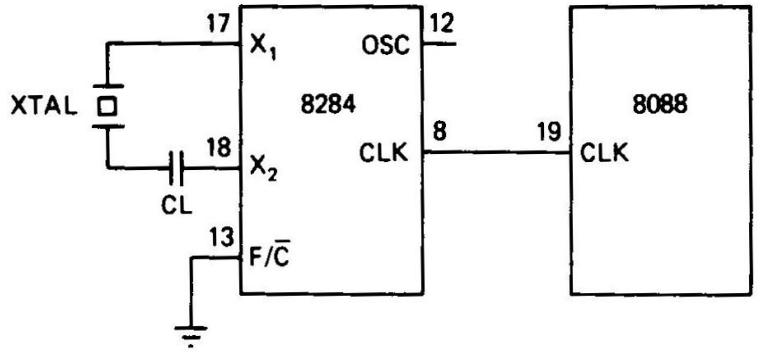

Figure 8–11 Connecting the 8284 to the 8088. (Reprinted with permission of Intel Corporation, © 1979)

8.7 BUS CYCLE AND TIME STATES

- A **bus cycle** defines the **sequence of events** when the MPU **communicates** with an external device, which starts with an **address** being output on the system bus followed by a **read or write data** transfer.