Chapter 8 Summary: The 8086 Microprocessor and its Memory and Input/Output Interface

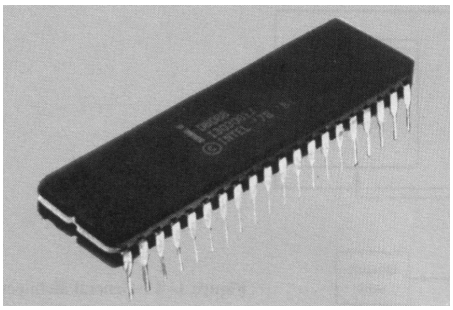

Figure 1-5 Intel Corporation's 8086 Microprocessor.

- The **8086**, announced in **1978**, was the **first 16-bit** microprocessor introduced by Intel Corporation.
- The **8086** is internally a **16-bit MPU** and **externally** it has a **16-bit data bus**. It has the ability to address up to **1 Mbyte** of memory via its **20-bit address bus**.
- In addition, it can address up to **64K of byte-wide input/output ports**.
- It is manufactured using **high-performance metal-oxide semiconductor (HMOS) technology**, and the circuitry on its chip is equivalent to approximately **29,000 transistors**.
- The 8086 is housed in a **40-pin dual in-line package**. The signals pinned out to each lead are shown in Fig. 8-1.
- The **address bus lines** A_0 through A_{15} and **data bus lines** D_0 through D_{15} are **multiplexed**. For this reason, these leads are labeled AD_0 through AD_{15}. By *multiplexed* we mean that the same physical pin carries an address bit at one time and the data bit at another time.

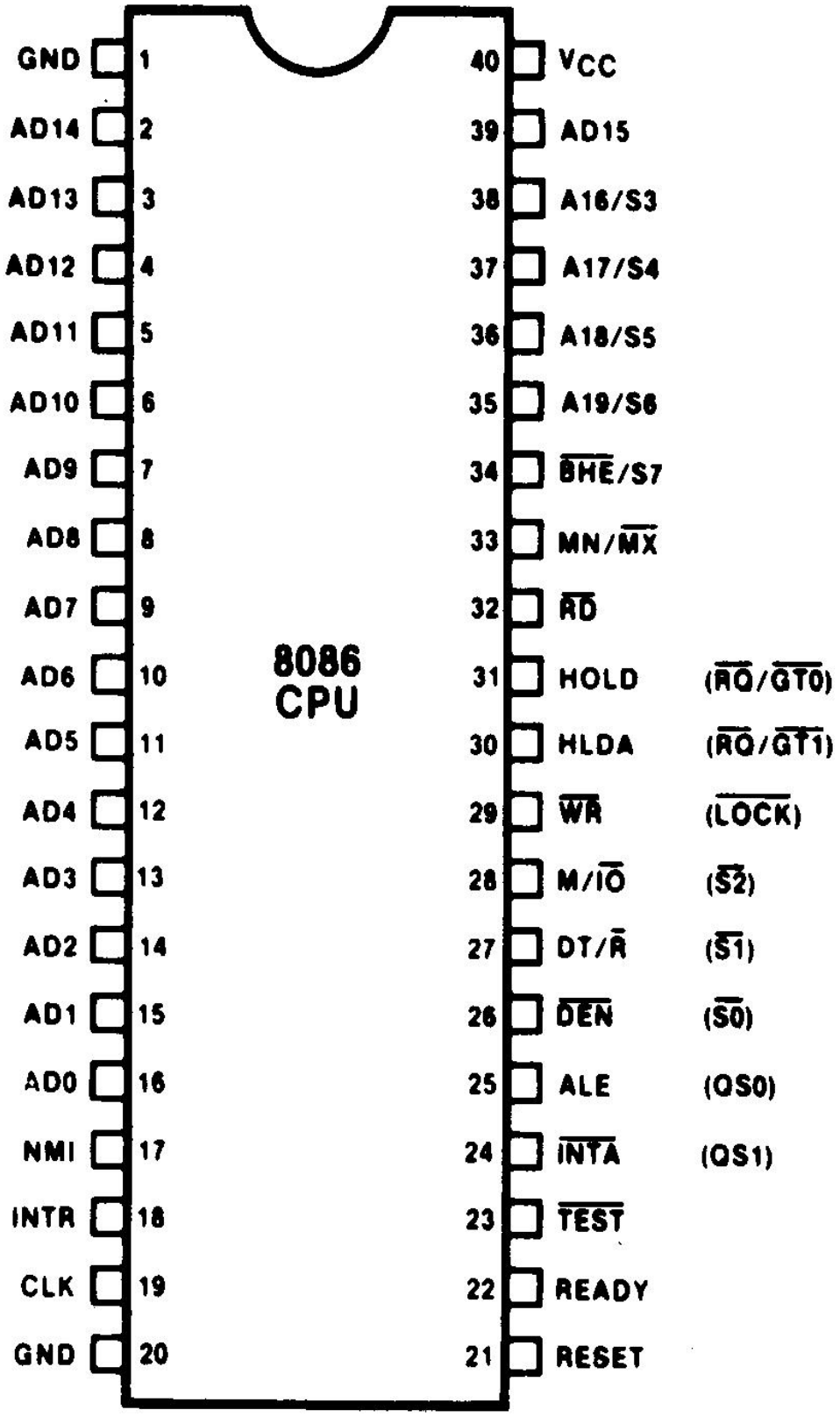

Figure 8-1 Pin layout of the 8086 Microprocessor.

8.2 MINIMUM-MODE AND MAXIMUM-MODE

- The **8086** can be configured to work in either of **two modes**:
- The **minimum mode** is selected by applying **logic 1** to the **MN/$\overline{\text{MX}}$** input lead. It is typically used for smaller **single microprocessor** systems.
- The **maximum mode** is selected by applying **logic 0** to the **MN/$\overline{\text{MX}}$** input lead. It is typically used for larger **multiple microprocessor** systems.
- Depending on the **mode** of operation selected, the **assignments** for a number of the **pins** on the microprocessor package are **changed**. The **pin functions** specified in **parentheses** pertain to the **maximum-mode**.
- We will **only** discuss **minimum-mode** operation of the 8086. In minimum mode, the **8086** itself **provides** all the **control signals** needed to implement the memory and I/O interfaces (see Fig. 8-3). In **maximum-mode**, a separate chip (the **8288 Bus Controller**) is used to help in sending control signals over the shared bus (see Fig. 8-5).

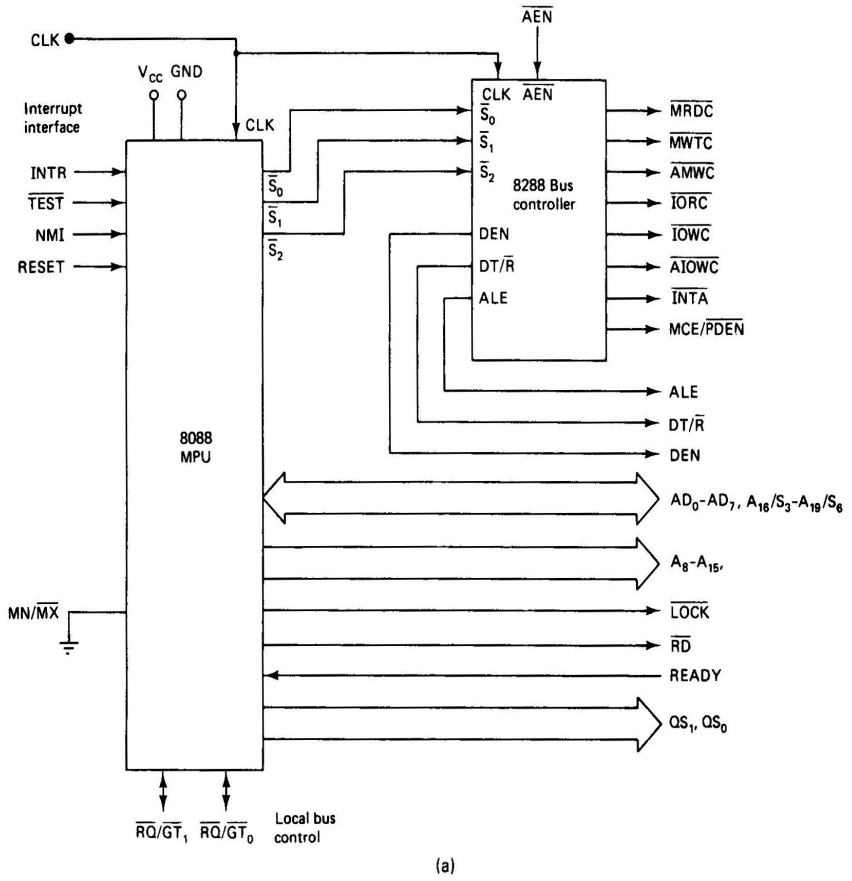

Figure 8–5 (a) 8088 maximum-mode block diagram. (b) 8086 maximum-mode block diagram.