NOTES ON THE FIELD EFFECT TRANSISTOR (FET)

The FET is a three terminal device like the BJT, but operates by a different principle. The three terminals are called the source, drain, and gate. The voltage applied to the gate controls the current flowing in the source-drain channel. No current flows through the gate electrode, thus the gate is essentially insulated from the source-drain channel. Because no current flows through the gate, the input impedance of the FET is extremely large (in the range of 10^{10}–10^{15} Ω). The large input impedance of the FET makes them an excellent choice for amplifier inputs.

The two common families of FETs, the junction FET (JFET) and the metal oxide semiconductor FET (MOSFET) differ in the way the gate contact is made on the source-drain channel.

In the JFET the gate-channel contact is a reverse biased *pn* junction. The gate-channel junction of the JFET must always be reverse biased otherwise it may behave as a diode. All JFETs are depletion mode devices—they are *on* when the gate bias is zero ($V_{GS} = 0$).

In the MOSFET the gate-channel contact is a metal electrode separated from the channel by a thin layer of insulating oxide. MOSFETs have very good isolation between the gate and the channel, but the thin oxide is easily damaged (punctured!) by static discharge through careless handling. MOSFETs are made in both depletion mode (*on* with zero biased gate, $V_{GS} = 0$) and in enhancement mode (*off* with zero biased gate).

In this class we will focus on JFETs.

Schematic symbols. Two versions of the symbols are in common use. The symbols in the top row depict the source and drain as being symmetric. This is not generally true. Slight asymmetries are built into the channel during manufacturing which optimize the performance of the FET. Thus it is necessary to distinguish the source from the drain. In this class we will use the asymmetric symbols found on the bottom row, which depict the gate nearly opposite the source. The designation *n*-channel means that the channel is *n* doped and the gate is *p* doped. The *p*-channel is complement of *n*-channel.

n-channel JFET   p-channel JFET

n-channel JFET   p-channel JFET
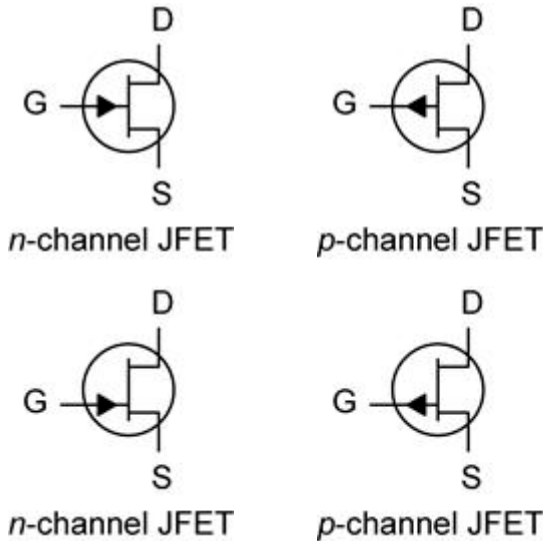
Common Nomenclature (*n*-channel FET example).
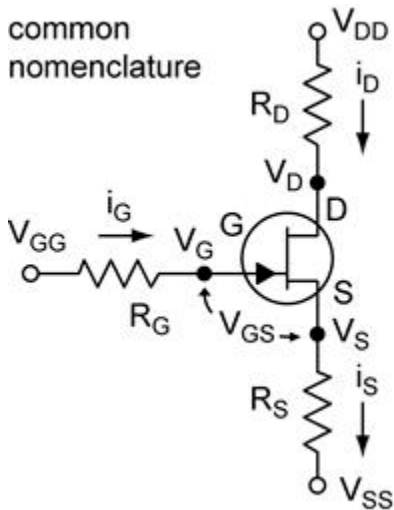
Regions of JFET operation:

Cut-off region: The transistor is off. There is no conduction between the drain and the source when the gate-source voltage is greater than the cut-off voltage. ($I_D = 0$ for $V_{GS} > V_{GS,off}$)

Active region (also called the Saturation region): The transistor is on. The drain current is controlled by the gate-source voltage (V_{GS}) and relatively insensitive to V_{DS}. In this region the transistor can be an amplifier. I_{DSS} is a parameter that is the maximum drain current, which occurs when the $V_{GS} = 0$. (The drain current with source shorted to the gate.)

In the active region:
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)^2$$

Ohmic region: The transistor is on, but behaves as a voltage controlled resistor. When V_{DS} is less than in the active region, the drain current is roughly proportional to the source-drain voltage and is controlled by the gate voltage.

$$I_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)\frac{V_{DS}}{-V_{GS,off}} - \left(\frac{V_{DS}}{V_{GS,off}}\right)^2\right]$$

$$R_{DS} \approx \frac{V_{GS,off}}{2I_{DSS}\left(V_{GS} - V_{GS,off}\right)} = \frac{1}{g_m}$$

Common Specifications.

I_{DSS} is the drain current in the active region for $V_{GS} = 0$. (I_D source shorted to gate)

$V_{GS,off}$ is the minimum V_{GS} where $I_D = 0$. $V_{GS,off}$ is negative for n-channel and positive for p-channel..

g_m is the transconductance, the change in I_D with V_{GS} and constant V_{DS}.

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{Ds}} = \frac{2I_{DSS}}{V_{GS,off}}\left(V_{GS} - V_{GS,off}\right)$$

Common Circuit Applications:

Voltage Controlled Switch. For the *on* state the gate voltage $V_{GS} = 0$ and for the *off* state $|V_{GS}| > |V_{GS,off}|$ (of greater magnitude than $V_{GS,off}$ and with the same sign). The sign of the voltage depends on the type of FET, negative for n-channel and positive for p-channel.
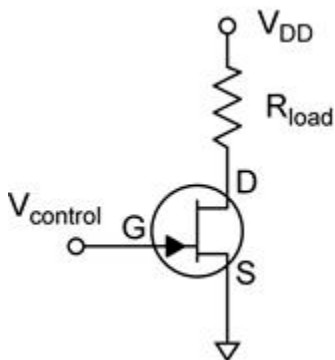

Current Source. The drain current is set by R_S such that $V_{GS} = -I_D R_S$. Any value of current can be chosen between zero and I_{DSS} (see the I_D vs V_{GS} graph for the JFET).
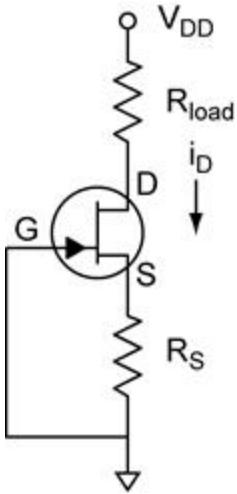
Source Follower. The simple source follower is shown below. The improved version is shown at the right. The lower JFET forms a current source. The result is that V_{GS} is held constant, removing the defects of the simple circuit.
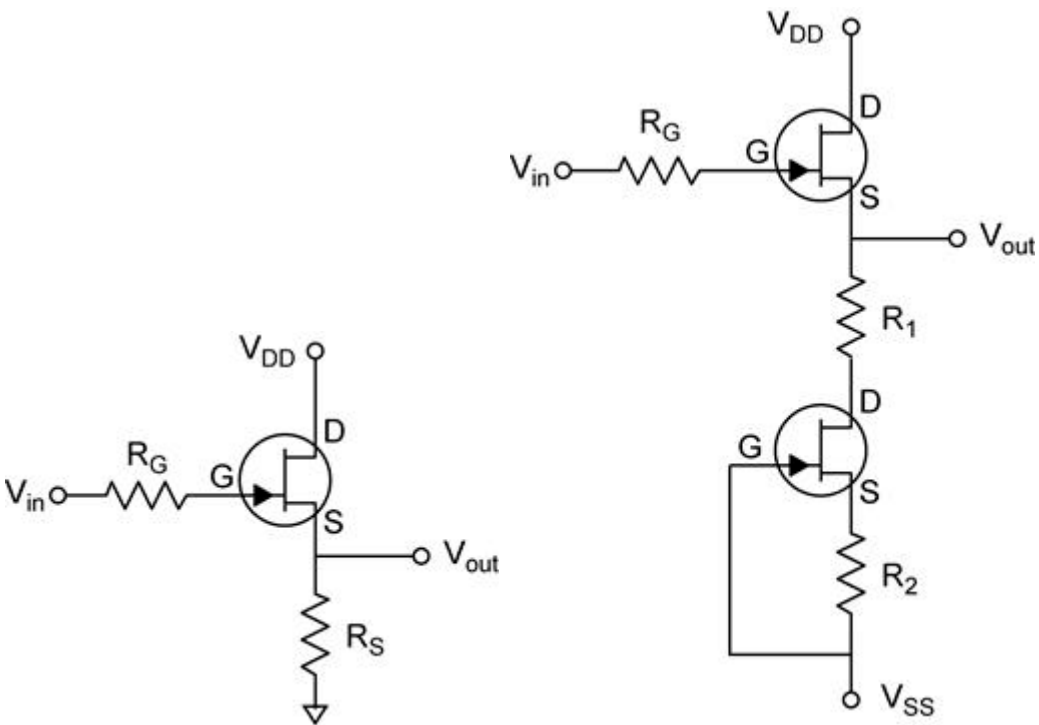
Voltage-Controlled Resistor. V_{GS} must be between zero and $V_{GS,off}$.
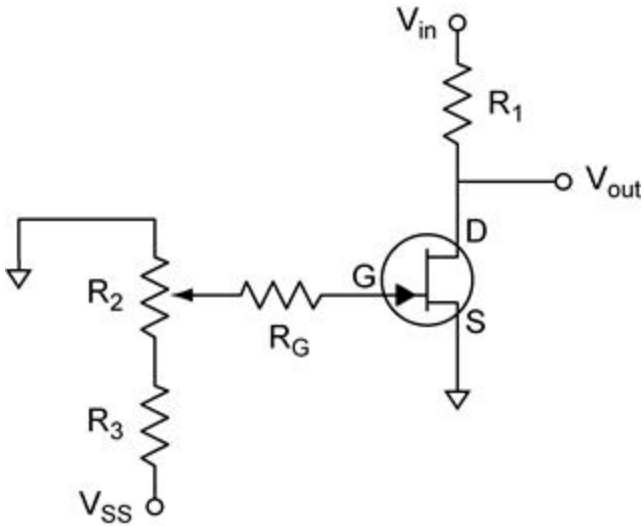
JFET Diode. The JET *pn* gate junction can be used as a diode by connecting the source and the drain terminals. This is done if very low reverse leakage currents are required. The leakage current is very low because the reverse leakage current scales with the gate area. Small gate areas are designed into JFETs because it decreases the gate-source and the gate-drain capacitances